UNITED STATES PATENT APPLICATION

FOR

POWER AMPLIFIER WITH DIGITAL POWER CONTROL AND ASSOCIATED METHODS

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POWER AMPLIFIER WITH DIGITAL POWER CONTROL AND ASSOCIATED METHODS

FIELD OF THE INVENTION

[01] This invention relates to the field of power amplifiers. In particular, this invention is drawn to controlling the output power of power amplifiers.

BACKGROUND OF THE INVENTION

[02] Power amplifiers, such as the types of power amplifiers used in wireless communication systems, must be capable of operating at various power levels based on instructions from a controller. A typical prior art power amplifier uses individual pins to control the various functions of the power amplifier. A typical power amplifier may receive signals relating to what band the power amplifier is operating in, and a control signal to control when the power amplifier turns on. A power amplifier may also receive an analog automatic power control signal APC having a power level proportional to the desired output power level.

[03] One problem with prior art power amplifiers is that the their functionality is limited. For example, limitations in the prior art prohibit some features, such as the ability to integrate new functions, or the ability for other devices to read the status of the power amplifier.

[04] Another problem in the prior art relates to controlling the output power of power amplifiers. When the designer of a wireless communication device (e.g., a cellular phone) implements any particular power amplifier with their design, a great amount of effort is required to design ramp profiles for use in controlling the output power of a power amplifier. The characteristics of a desired ramp profile depend on several factors including characteristics of the power amplifier being used, temperature, and battery voltage. As a result, designers typically must design new ramp profiles for every specific design.

SUMMARY OF THE INVENTION

[05] An RF power amplifier according to one illustrative embodiment of the invention includes power amplifier circuitry and memory formed using an integrated circuit. One or more ramp profiles are stored in the memory for use in setting the output power of the power amplifier. In one example, a digital interface is provided to allow a controller to control the output power of the power amplifier.

[06] Another illustrative embodiment of the invention provides a method of amplifying RF signals. One or more ramp profiles are stored using an integrated circuit. To control the output power of the power amplifier, one of the ramp profiles is selected.

[07] Other features and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description that follows below.

BRIEF DESCRIPTION OF THE DRAWINGS

[08] The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements and in which:

[09] FIG. 1 is a block diagram of a wireless system including a power amplifier and a serial interface.

[10] FIG. 2 is a diagram of a power amplifier formed on an integrated circuit.

[11] FIG. 3 is a schematic diagram illustrating the filter used on control signal pins.

[12] FIG. 4 is a schematic illustrating a blocking gate circuit.

[13] FIG. 5 is a schematic diagram illustrating how the serial digital output pin is driven.

[14] FIG. 6 is a schematic diagram of three of the power amplifier pins illustrating how the reference VDD is supplied.

[15] FIG. 7 is a schematic diagram of the buffer amplifier used for driving the SDO output signal.

[16] FIG. 8 is a block diagram of a prior art cellular phone power amplifier and controller.

[17] FIG. 9 is a block diagram of a power amplifier design of the present invention.

[18] FIG. 10 is a block diagram of a power amplifier of the present invention incorporated on a single chip.

[19] FIG. 11 is a block diagram of one example of clock generator circuit.

[20] FIG. 12 is a diagram of an exemplary power ramp.

[21] FIG. 13 is a block diagram of a power amplifier implemented as a module with multiple chips.

DETAILED DESCRIPTION

[22] In order to provide a context for understanding this description, the following description illustrates one example of a typical application of the present invention. A power amplifier using power control techniques of the present invention may be used for any desired applications, including a wireless transmission system such as mobile or cellular communication devices or other wireless devices. In a wireless device, the wireless device may include a transceiver, an antenna duplexer, and an antenna. Coupled between the transceiver and the antenna duplexer is an RF power amplifier for amplifying signals for transmission via the antenna. In the case of a wireless telephone application, the invention may be applied to GSM, CDMA, PCS, DCS, etc., or any other wireless systems. This is just one example of an application of a power amplifier utilizing the present invention. The invention may also be used in any other application requiring a power amplifier.

[23] In general, the present invention provides an RF power amplifier that is capable of being controlled digitally. In one example, a power amplifier is formed using an integrated circuit. The power amplifier includes a digital interface capable of receiving control information from an external controller. A plurality of ramp profiles are stored in memory on the integrated circuit and are selectively used to control the output power of the power amplifier depending on the desired output power level. The selection of a ramp

profile may also take into account information from sensors on the integrated circuit and/or from other parts of the RF device.

[24] The digital interface mentioned above may be take the form of a serial interface. The following description, and FIGS. 1-7, illustrate examples of how a serial interface may be provided to a power amplifier. The serial interface provides the power amplifier with increased flexibility, without the requirement for additional pins. As mentioned above, typical prior art power amplifiers are controlled using a few individual, dedicated pins.

[25] In contrast, with the present invention, the power amplifier is coupled to a serial interface to receive most of its instructions. FIG. 1 is a block diagram of a wireless system having a power amplifier 10, baseband controller 12, and transceiver 14. A serial interface 16 is coupled to the power amplifier 10, baseband controller 12, and transceiver 14. In one example, the serial bus used with the present invention is similar to an I^2C type bus. The baseband controller 12 controls the operation of both the transceiver 14 and power amplifier 10 over the serial interface 16. In addition, the power amplifier 10 also receives PAEN and APC signals from the baseband controller 12. In one example, the power amplifier 10 is integrated in a CMOS chip, which allows many functions to be integrated within the power amplifier. One example of a power amplifier integrated in a CMOS chip is described in commonly-owned US Patent No. 6,549,071, issued on April 15, 2003, entitled "POWER AMPLIFIER CIRCUITRY AND METHOD USING AN INDUCTANCE COUPLED TO POWER AMPLIFIER SWITCHING DEVICES," which

is expressly incorporated by reference herein. For example, the power amplifier can include temperature sensors, digital thermometers, battery sensors, and load conditioning sensing. These functions may use multiple bits of data, which can be communicated with the baseband controller 12 via the serial interface 16.

[26] The power amplifier serial interface provides several advantages over the prior art. First, the serial interface allows many bits to be communicated without using additional pins. Also, the power amplifier can share an existing bus in the system (like in the example shown in FIG. 1), or use a separate bus. If a bus is shared, a controller can provide a single instruction that can be received by the power amplifier, as well as other systems or components coupled to the bus. For example, if the controller sends a mode command to the transceiver, the power amplifier can "snoop" or monitor the bus to automatically determine which mode it should be in. The serial interface can also enable additional features, such as digital power control. In addition to a serial bus, other types of interfaces can also be used. For example, a parallel interface could be used with the power amplifier of the present invention, although more pins would be used.

[27] The power amplifier of the present invention is backwards compatible with systems that do not have a serial bus to communicate with the power amplifier. The power amplifier can operate in either a direct "pin mode" or in the "serial interface mode" when using the serial bus. Another advantage of the present invention is that some of the same pins function during the pin mode or the serial interface mode. FIG. 2 is a diagram of a power amplifier 10 formed on an integrated circuit, showing several of its pins. The

MODE pin is used to select the pin mode or the serial interface mode. The PAEN (power amplifier enable) pin is used to communicate to the power amplifier 10 when to turn on. The remaining pins shown in FIG. 2 designate two functions depending on which mode is selected (i.e., serial mode/pin mode).

[28] In pin mode, a standard pin interface is provided to allow programming of the power amplifier 10. A first input pin, BSEL (band select) is used to communicate to the power amplifier which band is being used (e.g., GSM or DCS). A second input pin, VDD is a reference voltage for the digital I/O and allows a user to set the digital I/O levels to be compatible with the baseband I/O levels. A first output pin, TLIMIT (thermal limit signal) triggers if the die temperature exceeds a predefined temperature limit. A second output pin, SHUTD (shutdown) triggers when the thermal limit threshold is crossed. The power amplifier will automatically shut down on the rising edge of SHUTD to protect the power amplifier from damage.

[29] In serial interface mode, a serial port is employed to allow programming of the power amplifier 10. If desired, the serial port can be shared with other devices (e.g., a transceiver, etc.) in addition to the baseband controller. The serial port allows access to certain features and internal registers that are not available in the pin control mode. A first input pin, SCLK (serial clock) receives the serial clock signal. A second input pin, SENB (serial enable) controls when the serial port is enabled. A third input pin, SDI (serial data out) is the serial data input pin. An output pin, SDO (serial data out) is the serial data output pin.

[30] One example of a feature that is enabled by the serial interface relates to thermal protection. In serial interface mode, a user may access programmable registers associated with thermal protection. If the die temperature exceeds a predetermined temperature setting, the baseband controller is alerted via the TLIMIT pin. If the die temperature exceeds a predetermined temperature, the power amplifier is automatically powered down to prevent device damage. These conditions may be detected by the baseband controller by monitoring the serial bus.

[31] There are several design issues that should be considered in implementing a serial bus in an RF power amplifier. For example, bus noise can cause spurs in the RFO frequency spectrum. Another issue is that during an RF burst, large voltages and currents at the RF carrier frequency can be induced in the serial bus lines causing loss and potential problems in logic circuits in the transceiver and baseband controller. Another issue is that high speed I/O's have electrostatic discharge (ESD) issues. Another issue relates to the number of pins needed to implement the serial interface. The following discusses design considerations relating to those issues.

[32] As mentioned above, bus noise can cause spurs in the power amplifier output RFO frequency spectrum. The present invention disables the serial bus during RF bursts. With the serial bus used with the present invention, the serial clock (SCLK) operates when data is being transferred, which happens between bursts.

[33] To address large voltages and currents induced at the RF carrier frequency during the RF burst, the present invention uses several approaches. For slower control signals (e.g., PAEN) a filtering circuit is used. FIG. 3 is a schematic diagram illustrating the filter used on slower control signal pins. In FIG. 3, signals sent to the PAEN pin are filtered by a low pass RC filter comprised of resistor R1 and capacitor C1. The filtered signal is connected between V_{BATT} and ground via diodes D1 and D2. The filtered signal is then inverted twice by inverters 18 and 20 to provide the internal power amplifier enable signal PAEN-CHIP. The signal PAEN is the signal that enables the power amplifier and is active during the entire burst. This signal is not used to communicate high speed digital data, so the low pass filter can be used to remove the RF pickup.

[34] For the faster signals (e.g., SCLK, SENB, SDI), the present invention uses a blocking gate that is enabled during the RF burst. FIG. 4 is a schematic illustrating a blocking gate circuit. FIG. 4 shows the non-filtered gate block circuit that is used with the serial clock SCLK signal. As shown, the SCLK signal passes through resistor R2, and is coupled between V_{BATT} and ground via diodes D3 and D4. The signal is then provided as a first input to NAND gate 22. A second input of NAND gate 22 is coupled to the inverted power amplifier enable signal $\overline{\text{PAEN - CHIP}}$, which is low during a burst. The output of the NAND gate 22 is inverted by inverter 24, to provide the internal serial clock signal SCLK-CHIP. During a burst, the signal SCLK-CHIP will always be high, essentially disconnecting the input signal SCLK. This same technique is used on other

high speed bus input signals SENB and SDI, preventing logic glitches and power supply current.

[35] During a burst, the serial data output pin is dealt with differently. The output is not filtered in the same way described above because of the amount of current that is driven. Instead, a driver is provided to drive either a "1" or a "0". FIG. 5 is a schematic diagram illustrating how the serial digital output pin is driven. Generally, a tri-state driver is provided so that, when an output signal is being driven between bursts, the driver drives a "1" or a "0." During a burst, and when a read-back is not occurring, the pin is tri-stated and a bias signal is applied to it.

[36] As shown in FIG. 5, the inverted power amplifier enable signal $\overline{\text{PAEN}}$ and the bus enable (ENABLE) signal are provided as inputs to AND gate 25. The output of AND gate 25 ($\overline{\text{PAEN}}$ & ENABLE) is coupled to an input of NAND gate 26, and to an input of NOR gate 28, after being inverted by inverter 30. During a burst, when $\overline{\text{PAEN}}$ is low and ENABLE is high, the outputs of NAND gate 26 and NOR gate 28 will be "1" and "0," respectively, regardless of the signal at SDO. As a result, switching devices M1 and M2 will both be off during a burst, making node 32 (which is also SDO) tri-stated. FIG. 5 also shows a low current bias circuit, comprised of switching devices M3, M4, and M5, which is connected to node 32 during a burst.

[37] The bias circuit biases the node 32 to $V_{DD}/2$ during the burst. As a result, the RF voltage pickup signal will appear across the tri-state devices and will not turn on the

parasitic diodes to ground and V_{BATT}, which reduces loss and reduces the RF voltage present on the digital line. In other words, during bursts, a goal is to keep diodes turned off while maximizing the impedance seen looking into the output pin SDO. Between bursts, when $\overline{PAEN}$ is high and the driver is enabled, the outputs of NAND gate 26 and NOR gate 28 will both be the inversion of SDO, which makes node 32 (or SDO at the output of the chip) equal to the value of SDO. Also, when $\overline{PAEN}$ is high, switching device M3 will be off so the bias circuit will not be applied to node 32. It is desirable when designing the power amplifier integrated circuit to choose the output pin SDO to be the pin on the package to be the pin with reduced pickup.

[38] As mentioned above, the high speed I/O's have ESD issues. To help reduce the RF current in the I/O loops, a series resistor (e.g., resistor R2 in FIG. 4) is used, and the capacitance at the inputs is reduced. However, the use of the series resistors can cause low ESD performance since a discharge can cause high current in the resistor, resulting in thermal damage. There is a trade-off when choosing the size of the resistor since a larger area resistor will have better ESD performance, but will have a higher capacitance. One suitable example for the series resistor is a 3 kohm poly resistor, which will have a relatively good RF performance and will meet 200 V ESD.

[39] It is desirable that the serial interface of the present invention have as few pins as possible due to the RF issues described above. In addition, it is desirable that the serial port interface also work in pin mode to be backwards compatible with existing power amplifiers. In addition, the digital interface levels are different (lower) than the battery

voltage. As a result, a reference V_{DD} is supplied, and level shifters are used at the inputs and outputs.

[40] As described above with respect to FIG. 2, four of the power amplifier pins function under either the pin mode or the serial interface mode. As described above, in the serial interface mode (when the MODE pin is high), the pins define a serial interface using pins SDI, SDO, SENB, and SCLK. When MODE is high, the MODE pin is used as the V_{DD} for the input and output level shifters (described below). In the pin control mode (MODE is low), the pins are defined as a pin control using pins BSEL, TLIMIT, and SHUTD. In this case, the SDI/VDD pin should be connected to V_{DD} which provides the supply for the input/output level shifters.

[41] FIG. 6 is a schematic diagram of three of the power amplifier pins illustrating how the number of pins are minimized, and how the reference V_{DD} is supplied. First, looking at the MODE pin, filter circuitry (resistor R3 and capacitor C2) is provided similar to that shown in FIG. 3. When MODE is high (serial interface mode), then the filtered signal is inverted twice by inverters 40 and 42. The outputs of inverters 40 and 42 each control a switch S1 and S2, respectively.

[42] In serial interface mode, switch S1 will be open and switch S2 closed, which causes the voltage at pin MODE to become the internal reference power supply (INP-VDD). As shown, INP-VDD supplies NAND gates 44 and 46, as well as inverters 48 and 50. Since the MODE signal comes from the baseband controller, the internal reference

power supply will be compatible with the baseband controller voltage levels. Pins SDI and SENB include circuits similar to the circuit shown in FIG. 4. The signals pass through resistors R4 and R5, and then through the NAND gates 44 and 46, between bursts. During bursts, the outputs of the NAND gates 44 and 46 will be constant, regardless of the signals at the SDI and SENB pins. FIG. 6 also shows level shifters 52 and 54 which shift the signal level to the V_{BATT} level. The level shifters are comprised of switching devices M6 through M13 and inverters 56 and 58. In pin mode, switch S1 will be closed and switch S2 will be open. In pin mode, the internal voltage supply INP-VDD will no longer be equal to the voltage on the MODE pin.

[43] Another feature of the present invention relates to how the serial output signal at SDO is driven. Since the signal on the SDO pin is provided to the baseband chip, it is desirable for the voltage level to be compatible with the level at the baseband chip. However, it may be impractical to pull much current from INP-VDD, which is provided by the MODE pin. To solve this problem, a buffer amplifier is used when transmitting a signal over the serial bus. FIG. 7 is a schematic diagram of the buffer amplifier used for driving the SDO output signal. FIG. 7 is similar to what is shown in FIG. 5, with the addition of op-amp 60, which buffers INP-VDD to provide the drive. The buffer circuitry allows more current to be drawn from the battery, rather than from INP-VDD. Since the op-amp 60 consumes power when enabled, it is enabled when the user requests a read-back through the serial interface. When the user is not requesting a read back, SDO is tri-stated.

[44] As mentioned above, a serial interface enables several features, including digital power control. To better understand the power control functions of the present invention, following is a description of how output power is controlled in typical prior art power amplifiers. FIG. 8 is a block diagram of a prior art mobile phone power amplifier and controller. FIG. 8 shows a power amplifier 70 having an RF input RFI and an RF output RFO, which is connected to an antenna 72. A directional coupler 74 senses the output power provided to the antenna for use in a feedback loop. A power detector comprised of diode D5 and capacitor C2 create a feedback signal 78, which is provided as one input to an op-amp 80. A baseband controller 82 includes a digital to analog converter (DAC) which generates an analog power control signal APC that relates to a desired output power level. The signal APC is provided as a second input to the op-amp 80. The op-amp 80 compares the feedback signal 78 and APC to generate a power control signal 86, which controls the output power level of the power amplifier 70. In this prior art system, multiple integrated circuits are used to implement the system, and the signals between chips are analog. This type of design provides a challenge to designers who must implement good layout and part placement, since noise and un-wanted signals coupling into the analog signals can cause problems.

[45] An improved interface is described above with respect to FIGS. 3-9. A power amplifier system using the improved interface and the power control techniques (described below) can be implemented in a single chip design, or in a multi-chip module.

[46] FIG. 9 is a block diagram of a single chip power amplifier design of the present invention. FIG. 9 shows a power amplifier 90 having an input RFI and an output RFO connectable to an antenna (not shown). The digital interface is connected to logic circuitry 92, such as circuitry described above with respect to FIGS. 3-9. The digital interface is connectable to a baseband controller (not shown) to provide communication with the baseband controller. The logic circuitry 92 is connected to digital to analog converter (DAC) circuitry 94. When the baseband controller sends information relating to a desired output power level, the DAC 94 generates a power control signal 96, which controls the output power of the power amplifier 90.

[47] FIG. 10 is a more detailed block diagram of a power amplifier formed on a chip 98. In one example, the chip is implemented in CMOS, although other technologies could also be used. In this example, a digital signal processor engine (DSP) 100 is incorporated into the chip 98. The DSP 100 generates or selects ramp profiles based on information coming from a baseband controller (not shown) over the digital interface. When the DSP 100 selects a ramp profile, the DAC 94 will convert the profile into an analog power control signal, which is filtered by low pass filter 102 to generate analog power control signal APC 96, which controls the output power of the power amplifier 90. The DSP 100 runs during the RF bursts and should be designed for low noise so it does not cause spurs at output RFO.

[48] The DSP 100 is clocked from a clock signal (CLOCK) that is generated by clock generator 104. FIG. 11 is a block diagram of one example of clock generator 104. FIG.

11 shows a divider 104 the divides the RF input signal RFI to generate the clock signal CLOCK. Since the DSP 100 and DAC 94 run during the power amplifier burst, they are be designed such that they do not create RF spurs at the power amplifier output. In another example, a clock signal is provided externally to a pin on the chip 98.

[49] Referring back to FIG. 10, a user of the power amplifier chip 98 can use the the digital interface to download desired ramp profiles. Also, multiple ramp profiles can be stored in an on-chip RAM 112 and/or ROM 114. The power amplifier is also capable of using one or more sensors 116 when controlling the output power level. For example, the temperature of the power amplifier can be sensed and used when selecting a ramp profile. In another example, the battery voltage can be sensed and used to select the appropriate ramp profile. Also, the DSP 100 can generate ramp profiles based on an internal algorithm, while taking into account one or more variables (e.g., required power, temperature, battery voltage). Sensors can also be used to sense other conditions, if desired. Whether a ramp profile is selected or created, the profile can be scaled according to the desired power level the user programs.

[50] The power control technique of the present invention provides several advantages over the prior art. First, the digital interface makes the power amplifier very easy to use and to design into a system. Also, as a result of the internal sensors, more optimum ramp profiles can be used than are possible in the prior art. And, since the entire power control and ramping is integrated with the power amplifier in one part, complex algorithms can be used to give optimum ramp performance, while having an easy to use and program

part. Another advantage of the present invention relates to testing the power amplifier. Since the ramp profiles and control algorithms are contained in the power amplifier, the power amplifier can be tested without having to build the entire system with which it is used.

[51] To help illustrate the value of some of these advantages, following is background information relating to the design of power ramp profiles. When designing ramp profiles, there are requirements for meeting time domain power masks and spectral frequency domain masks over a range of temperatures, battery voltages, and power levels. FIG. 12 is a diagram of an exemplary power ramp. FIG. 12 shows a power ramp 120 and an example of a time domain power mask 122. Typically, a modified raised cosine function is used to create the power ramp. When designing power ramps, they should fall within the time domain mask and the frequency domain mask, as defined by the relevant specifications. In typical prior art systems, the power ramp profile is designed by a system designer and is contained in the baseband DSP chip. The ramp profile typically is highly dependent on the particular power amplifier used. Therefore, system designers go through this process for every design, or for every power amplifier used. In contrast, with the present invention, the complete power ramping function is integrated in the power amplifier andwill largely be the same for various applications.

[52] Following is one example of how a power amplifier is controlled in one possible implementation. First, the baseband controller writes to a digital register in the power amplifier (via the digital interface) to set the desired output power. When a burst is

desired, the baseband chip raises the PAEN signal. When PAEN goes high, the power amplifier DSP will select and scale a ramp profile stored in memory based on the desired power level, and on sensors such as temperature and battery voltage. To help minimize noise, the ramp can be pre-computed between bursts and stored in memory, so that during the burst, the data is read and presented to the DAC to generate the analog internal APC signal.

[53] Since the entire ramp generation is included on the power amplifier chip, the ramp profiles can be designed by the power amplifier designers and stored in the power amplifier ROM. One factor that will vary from different applications designs is the loss associated with the antenna switch module and the antenna. To compensate for this loss, a user can program an internal power amplifier register with this loss, and the power amplifier DSP can compensate correctly for the loss. In this example, a user (i.e., someone designing a system that uses the power amplifier of the present invention) would need merely to program the antenna loss factor, the desired output power, and use PAEN to enable the power amplifier. Therefore, there would be no need for the user to create power ramp profiles.

[54] While the digital power control techniques of the present invention have been described with respect to a power amplifier implemented using a single chip, other variations are also possible. FIG. 13 is a block diagram of a power amplifier implemented as a module containing multiple chips. FIG. 13 shows a power amplifier module 124. The module 124 includes a printed circuit board 126 and a plurality of chips mounted to the

circuit board or substrate 126. A power amplifier chip 128 contains the power amplifier circuitry. In the example shown, the power amplifier chip 128 is implemented in GaAs. A CMOS controller chip 130 is also mounted to the board 126 and contains the control circuitry for the power amplifier. Referring to FIG. 10, the controller chip 130 may contain all of the components shown in FIG. 10, except for the power amplifier. The functionality of the power amplifier module 124 is substantially the same as that described above.

[55] In the preceding detailed description, the invention is described with reference to specific exemplary embodiments thereof. Various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.